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EXAMINER

TRUJILLO, JAMES K

ART UNIT PAPER NUMBER

2116

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/20/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/751,372

Applicant(s)

KOERTZEN ET AL.

Examiner

James K. Trujillo

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 December 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4, 7-11, 13, 16-29, 31, 33-35, 37 and 38 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

- 5) ☐ Claim(s) _____ is/are allowed.

- 6) ☒ Claim(s) 1-4, 7-11, 13, 16-29, 31, 33-35, 37, and 38 is/are rejected.

- 7) ☐ Claim(s) _____ is/are objected to.

- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment dated 10/02/06
2. Claims 1-4, 7-11, 13, 16-29, 31, 33-35, 37, and 38 are presented for examination. Applicant has canceled claims 5, 6, 12, 14, 15, 30, 32 and 36.

Claim Objections

3. Claims 13, 31, 37 and 38 objected to because of the following informalities:
 - a. Claims 13, 31, 37 and 38 dependent upon claims that have been canceled. For examination purposes it will be interpreted that the claims 13, 31, 37 and 38 are dependent on the same claim as the corresponding canceled claim.Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 1-4, 7-11, 13, 16-29, and 31 are rejected under 35 U.S.C. 102(a) as being anticipated by Hsu et al., U.S. Patent Application Publication 2004/0003310.
6. Regarding claim 1, Hsu teaches an apparatus comprising:
 - a. a first device (voltage regulator 210, figure 2) to receive (paragraph [0013]) a first signal from an integrated circuit (IccID/VccID signal is sent from a processor to indicate the amount of current required, paragraphs [0013], [0017] [0029], [0032] and [0033])

representing a first supply voltage value (the voltage regulator determines an appropriate slope of the load line thereby necessitating a determining a voltage based on the I_{ccID} therefore the I_{ccID} represents a supply voltage; in the case where V_{ccID} is used, it represents a voltage value), a first supply current value associated with the first supply voltage value (the slope requires that current be associated with the first supply voltage value, figure 3), and a second supply voltage value, and a second supply current value associated with the second supply voltage (in order to determine a load line the signal would have to represent a first voltage associated with a first current and a second voltage associated with a second current, paragraph [0013], [0029], [0032] and [0033] and figure 2; a slope of a load line requires at least two voltage values and two current values), and

b. to output an output supply voltage to the integrated circuit based on the first signal (operating the voltage regulator according to the load line, paragraph [0033] and block 430, figure 4).

7. Regarding claim 2, Hsu taught the apparatus according to claim 1, as described above.

Hsu further teaches wherein the first signal represents an impedance value (the first signal of Hsu represents a load line which inherent represents an impedance value as its slope, figures 1 and 3).

8. Regarding claim 3, Hsu taught the apparatus according to claim 1, as described above.

Hsu further teaches the first device to adjust the output supply voltage to a value based at least in part on the first signal (the voltage regulator of Hsu supplies V_{cc} according to the load line, paragraphs [0004] and paragraphs [0034]).

9. Regarding claim 4, Hsu taught the apparatus according to claim 3, as described above.

Hsu further teaches the first device comprising: a voltage regulator converter to generate the

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output supply voltage (controller/driver 211, figure 2); and a voltage regulator converter to receive the first signal and to transmit a control signal to the voltage regulator converter, the control signal to control the value of the supply voltage (controller/driver 211, figure 2).

10. Regarding claim 7, Hsu taught the apparatus according to claim 1, as described above.

Hsu further teaches wherein the output supply voltage is associated with an output supply current, wherein the first supply voltage value and the first supply current value define a first coordinate of a voltage vs. current coordinate system (signal of Hsu defines load line 302 having a first coordinate, figure 3), wherein the second supply voltage value and the second supply current value define a second coordinate of the voltage vs. current coordinate system (signal of Hsu load line 302 having a second coordinate, figure 3), wherein the first coordinate and the second coordinate define a line (load line 302, figures 3), wherein the value of the output supply voltage and a value of the output supply current define a third coordinate (an operating point of the voltage regulator along the load line), and wherein the line substantially comprises the third coordinate (an operating point along a load line inherently comprises a third coordinate).

11. Regarding claim 8, Hsu taught the apparatus according to claim 1, as described above.

Hsu further teaches wherein the first signal represents a slope of a power supply load line (load line 302 inherently has a slope, figures 3).

12. Regarding claims 9-11, 13, 16-21, and 27-29, Hsu taught claimed apparatus for receiving a first signal therefore he also teaches the claimed methods for receiving and transmitting a first signal and the claimed apparatus for transmitting the first signal.

13. Regarding claim 22, Hsu taught the apparatus according to claim 16, as described above.

Hsu taught further comprising: receiving a second signal representing a third supply voltage

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value associated with the first supply current value, and representing a fourth supply voltage value associated with the second supply current value (another signal representing load line 301, figures 3).

14. Regarding claim 23, Hsu taught the apparatus according to claim 22, as described above. Hsu further teaches wherein the second signal represents a second impedance value (load line 301 inherently represent a second impedance value, figures 3).

15. Regarding claim 24, Hsu taught the apparatus according to claim 22, as described above. Hsu further teaches wherein the second signal represents a slope of a second power supply load line (load line 301 represent a slope of a second power supply load line).

16. Regarding claim 25, Hsu taught the apparatus according to claim 22, as described above. Hsu further teaches further comprising: adjusting the output supply voltage to a value based at least in part on the second signal (supplying voltage from the voltage regulator according to load lines 310, figures 3).

17. Regarding claim 26, Hsu taught the apparatus according to claim 25, as described above. Hsu further teaches wherein the second output supply voltage is associated with a second output supply current, wherein the third supply voltage value and the first supply current value define a first coordinate of a voltage vs. current coordinate system, wherein the fourth supply voltage value and the second supply current value define a second coordinate of the voltage vs. current coordinate system, wherein the first coordinate and the second coordinate define a line, wherein the value of the second output supply voltage and a value of the second output supply current define a third coordinate, and wherein the line substantially comprises the third coordinate (load

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line 301 defines a first load line and load line 302 defines is a second load line, figure 3; each load line requires two voltages and two currents).

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

19. Claims 33-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al., U.S. Patent Application Publication 2004/0003310 in view of Microsoft Computer Dictionary (Microsoft).

20. Regarding claim 33, Hsu teaches a system comprising:

- a. a microprocessor to transmit a first signal representing a first supply voltage value, a first supply current value associated with the first supply voltage value, and a second supply voltage value, and a second supply current value associated with the second supply voltage value (the processor provides signals indicating amount of current under an operating condition, paragraphs [0013] and [0017]; also, IccID/VccID signal is sent from a processor to indicate the amount of current required, paragraphs [0013], [0017], [0029], [0032] and [0033]);
- b. a voltage regulator to receive the first signal (VR 150 figure 1, also voltage regulator 210, figure 2; IccID/VccID is provided to the voltage regulator, paragraph [0033]); and
- c. a memory electrically coupled to the microprocessor (Main Memory 115, figure 115).

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Hsu does not explicitly disclose wherein the memory is a double data rate memory.

Microsoft teaches a double data rate memory provides the advantage of doubling memory throughput (under definition of DDR SDRAM).

It would have been obvious to one of ordinary skill in the art, having the teachings of Hsu and Microsoft before them at the time the invention was made to modify the memory of Hsu to use the DDR SDRAM as taught by Microsoft.

One of ordinary skill in the art would have been motivated to make this modification in order to obtain the advantage of doubling memory throughput in view of the teachings of Microsoft.

21. Regarding claim 34, Hsu together with Microsoft taught the system according to claim 33, as described above. Hsu further teaches wherein the first signal represents an impedance value (the current will determine the impedance value for a given regulator output voltage, paragraph [0017]).

22. Regarding claim 35, Hsu together with Microsoft taught the system according to claim 33, as described above. Hsu further teaches wherein the first signal represents a slope of power supply load line (the voltage regulator determines a load line based on the signal, therefore it represents the slope of a load line, paragraph [0013]).

23. Regarding claim 36, Hsu together with Microsoft taught the system according to claim 33, as described above. Hsu further teaches wherein the voltage regulator to adjust a supply voltage to a value based at least in part on the first signal (voltage regulator will supply voltage according to a load line, paragraph [0013]).

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24. Regarding claim 37, Hsu together with Microsoft taught the system according to claim 33, as described above. Hsu further teaches the voltage regulator comprising:
- a. a voltage regulator converter to generate the output supply voltage (controller/driver 211, figure 2); and
 - b. a voltage regulator controller to receive the first signal and to transmit a control signal to the voltage regulator converter (from processor 201, figure 2), the control signal to control the value of the output supply voltage (controller/driver 211, figure 2; the voltage regulator is operated according to the load line, paragraph [0033]).
25. Regarding claim 38, Hsu together with Microsoft taught the system according to claim 33, as described above. Hsu further teaches wherein the output supply voltage is associated with an output supply current, wherein the first supply voltage value and the first supply current value define a first coordinate of a voltage vs. current coordinate system, wherein the second supply voltage value and the second supply current value define a second coordinate of the voltage vs. current coordinate system, wherein the first coordinate and the second coordinate define a line, wherein the value of the supply voltage and a value of the supply current define a third coordinate, and wherein the line substantially comprises the third coordinate (paragraph [0033] and 420 of figure 4).

Response to Arguments

26. Applicant's arguments, see pages 11-12, filed 10/2/06, with respect to 1-4, 7-11, 13, 16-29, and 31 have been fully considered and are persuasive. The rejections based on Horigan et al., U.S. Patent 6,566,848 of claims 1-4, 7-11, 13, 16-29, and 31 have been withdrawn.

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27. Applicant's arguments filed 10/2/06 with respect to claim 1-4, 7-11, 13, 16-29, 31, 33-35, 37, and 38 based on Hsu and rejections based on Hsu in view of Microsoft have been fully considered but they are not persuasive.

28. Applicant argues in substance that Hsu does not teach reception of a first signal from an integrated circuit, wherein the first signal represents a first supply voltage value, a first supply current value associated with the first supply voltage value, a second supply voltage value, and a second supply current value associated with the second supply value because the IccID signal of Hsu does not indicate a voltage associated with the maximum supply current Icc. The examiner respectfully disagrees. Applicant is directed to paragraphs [0017], [0027]-[0029] and figure 3. In Hsu the processor sends an IccID or a VccID (as the VccID may be used in a similar manner as the IccID in order to find the corresponding current) signal and the voltage regulator responds by sending an appropriate current and voltage. Specifically, the IccID signal is used to determine the Icc and Vcc at which the voltage regulator is to operate according to a particular load line as shown in figure 3. For any IccID a particular Icc and Vcc are selected according to a load line. The voltage regulator will operate at any point along the load line accordingly. As the operation changes the voltage regulator varies the current and voltage according to the particular load line. When the voltage regulator changes to operate at a new voltage and current it effectively operates at a new point on the load line. Therefore, Hsu does teach reception of a first signal from an integrated circuit, wherein the first signal represents a first supply voltage value, a first supply current value associated with the first supply voltage value, a second supply voltage value, and a second supply current value associated with the second supply value the IccID associates a first supply voltage value with a first supply current value (relating Vcc and


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Icc according to a load line). The load line has at least a second supply voltage and an associated second supply current value (because the load line represent multiple operating point according to Vcc and Icc).

Conclusion

29. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.


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